ABSTRACT

A method and apparatus for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit where scan chains embedded in a scan core 303 have no external access, such as the case when they are surrounded by pattern generators 302 and pattern compactors 305, using a DFT (design-for-test) technology such as Logic BIST (built-in self-test) or Compressed Scan. This invention includes an output-mask controller 301 and an output-mask network 304 to allow designers to mask off selected scan cells 311 from being compacted in a selected pattern compactor 305. This invention also includes an input chain-mask controller and an input-mask network for driving constant logic values into scan chain inputs of selected scan chains to allow designers to recover from scan chain hold time violations. Computer-aided design (CAD) methods are then proposed to automatically synthesize the output-mask controller 301, output-mask network 304, input chain-mask controller and input-mask network, and to further generate test patterns according to the synthesized scan-based integrated circuit.